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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/609,690
Filing Date: July 05, 2000
Appellant(s): WU ET AL.

Kevin J. Zilka
Registration No. 41,429
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 22, 2008 appealing from the Office action mailed August 23, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The Examiner relied upon Irwin, U.S. Patent No. 6,393,026, Kadambi, U.S. Patent No. 6,850,521, and Scales, U.S. Patent No. 5,761,729.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Irwin, U.S. Patent No. 6,393,026.

Irwin teaches the invention as claimed including a data packet processing system and method for a router which uses a packet switching software for routing data packets between data networks (see abstract).

Regarding claim 1, Irwin teaches an apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets (col. 5, lines 46-52, col. 6, lines 5-8, Irwin discloses a data packet processing system that forwards packets and assigns a program counter);

an addressable memory unit in which a plurality of instruction sets for packet processing are stored (col. 6, lines 5-8, Irwin discloses a data packet processing system);

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit (col. 6, lines 5-16, Irwin discloses a thread assigned to the packets that allows the forwarding program to process the packets); and

a data bus connecting the addressable memory unit and the first and second data processing units. (col. 8, lines 49-52, Irwin discloses a processor bus).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-16 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin in view of Kadambi, U.S. Patent No. 6,850,521.

Irwin teaches the invention substantially as claimed including a data packet processing system and method for a router which uses a packet switching software for routing data packets between data networks (see abstract).

As to claim 2, Irwin teaches the apparatus of claim 1, further comprising a table (col. 1, lines 32-57).

Irwin fails to teach the limitation further including a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein.

However, Kadambi teaches a method and apparatus for high performance switching of data packets in local area communications networks (see abstract). Kadambi discloses a rules engine attached to the FFP (col. 31, lines 20-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Irwin in view of Kadambi to use a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein. One would be motivated to do so because it allows for rules to be applied to the filtering of packets.

As to claim 3, Irwin teaches the apparatus of claim 1, further comprising a table (col. 1, lines 32-57).

Irwin fails to teach the limitation further including a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy.

However, Kadambi discloses a filtering logic in a rules table (col. 35, lines 57-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Irwin in view of Kadambi to use a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy. One would be motivated to do so because it allows for rules to be applied to the filtering of packets.

Regarding claim 4, Irwin and Kadambi teach the apparatus of claim 3, wherein at least one of said policies comprises:

a first address pointer element for identifying the location in said addressable memory unit of one of said plurality of instruction sets (col. 35, lines 57-64, Kadambi discloses logic 1411 in the FFP 141 which points to instruction sets to take action), and

a second address pointer element for identifying the location in said addressable memory unit of a state block (col. 31, lines 20-34, Kadambi discloses the FFP which is essentially a state machine).

Regarding claim 5, Irwin and Kadambi teach the apparatus of claim 3, wherein said first data processing unit assigns a thread to each said incoming packet, wherein

said thread corresponds to one of said policies stored in said policy action table (col. 35, lines 24-65, Kadambi).

Regarding claim 6, Irwin and Kadambi teach the apparatus of claim 3, wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table (col. 35, lines 24-65, Kadambi, col. 6, lines 5-16, Irwin).

Regarding claim 7, Irwin and Kadambi teach the apparatus of claim 6, wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread (col. 31, lines 20-34, col. 35, lines 24-65, Kadambi discloses the use of FIFO in the FFP).

Regarding claim 8, Irwin and Kadambi teach the apparatus of claim 6, wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet (col. 31, lines 20-34, col. 35, lines 57-64, Kadambi).

Regarding claim 9, Irwin and Kadambi teach the apparatus of claim 6, wherein said thread is assigned to said first incoming packet based on said first rule (col. 30, lines 54-61, col. 35, lines 24-65, Kadambi).

Regarding claim 10, Irwin and Kadambi teach the apparatus of claim 6, wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table (col. 35, lines 24-65, Kadambi discloses different rules used in the filtering logic).

Regarding claim 11, Irwin and Kadambi teach the apparatus of claim 10, wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread (col. 35, lines 24-65, Kadambi).

Regarding claim 12, Irwin and Kadambi teach the apparatus of claim 10, wherein said second thread is assigned to said second incoming packet based on said second rule (col. 35, lines 24-65, Kadambi).

Regarding claim 13, Irwin and Kadambi teach the apparatus of claim 3, wherein said first processing unit further comprises logic for matching a plurality of incoming

packets to a stored corresponding plurality of rules and for generating a thread for each packet that matches one of said plurality of rules, each said thread identifying the location of one of said at least one data processing policy in said policy action table (col. 35, lines 24-65, Kadambi).

Regarding claim 14, Irwin and Kadambi teach the apparatus of claim 13, wherein the second data processing unit is adapted to process each packet according to said data processing policy corresponding to said thread associated with said packet (col. 35, lines 24-65, Kadambi).

Regarding claim 15, Irwin and Kadambi teach the apparatus of claim 13, further comprising a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit (col. 31, lines 35-45, col. 35, lines 24-65, Kadambi discloses packets stored within FFP, col. 10, lines 5-17 in Irwin).

Regarding claim 16, Irwin and Kadambi teach the apparatus of claim 1, wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel (col. 5, lines 46-54, Kadambi discloses a plurality of modular systems on chip for parallel processing)

Regarding claim 30, Irwin and Kadambi teach an apparatus for processing data packets, comprising:

a first data processing unit adapted to filter incoming packets (col. 5, lines 46-52, col. 6, lines 5-8, Irwin);

an addressable memory unit in which a plurality of instruction sets for packet processing are stored (col. 6, lines 5-8, Irwin);

a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit (col. 6, lines 5-16, Irwin);

a data bus connecting the addressable memory unit and the first and second data processing units (col. 8, lines 49-52, Irwin).

Irwin fails to teach the limitation further including wherein a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy; wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table; wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread; wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used

by said first set of instructions for processing the first incoming packet; wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table; wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread; wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit; wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel; and wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output.

However, Kadambi discloses wherein a policy condition table connected to said first data processing unit, said policy condition table having a plurality of rules stored therein (col. 31, lines 20-34, Kadambi);

wherein a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy (col. 35, lines 57-64, Kadambi);

wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming

packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table (col. 35, lines 24-65, Kadambi);

wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread (col. 30, lines 54-61, col. 35, lines 24-65, Kadambi);

wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet (col. 31, lines 20-34, col. 35, lines 57-64, Kadambi);

wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table;

wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread (col. 35, lines 24-65, Kadambi, col. 6, lines 5-16, Irwin);

wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit (col. 5, lines 46-54, col. 31, lines 35-45, col. 35, lines 24-65, Kadambi; col. 10, lines 5-17, Irwin);

wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel (col. 5, lines 46-54, col. 31, lines 35-45, col. 35, lines 24-65, Kadambi; col. 10, lines 5-17, Irwin);

wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output (col. 31, lines 20-45, col. 35, lines 24-65, Kadambi).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Irwin in view of Kadambi to use a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy; wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table; wherein said second data processing unit is adapted to process the first incoming packet according to said data processing policy corresponding to said first thread; wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet; wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet

matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table; wherein said second data processing unit is adapted to process the second incoming packet according to said data processing policy corresponding to said second thread; wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit; wherein said second data processing unit comprising a plurality of general purpose processors for executing instructions in parallel; and wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output. One would be motivated to do so because it allows for rules to be applied to the filtering of packets.

5. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Irwin and Kadambi in view of Scales, U.S. Patent No. 5,761,729.

Irwin teaches the invention substantially as claimed including a data packet processing system and method for a router which uses a packet switching software for routing data packets between data networks (see abstract). Kadambi teaches the invention substantially as claimed including a method and apparatus for high performance switching of data packets in local area communications networks (see abstract).

As to claim 17, Irwin and Kadambi teach the method of claim 16.

Irwin and Kadambi fail to teach the limitation further including at least one said general purpose processor comprising a complex instruction set computer processor.

However, Scales teaches a distributed computer system including a distributed shared memory (see abstract). Scales shows evidence of the use of a complex instruction set computer processor (col. 1, lines 63-67; col. 2, lines 1-7, 49-67; col. 3, lines 1-8, 41-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Irwin and Kadambi in view of Scales to use a complex instruction set computer processor. One would be motivated to do so because a complex instruction set processor can perform several low-level operations and can deal with packet complexity.

As to claim 18, Irwin and Kadambi teach the method of claim 16.

Irwin and Kadambi fail to teach the limitation further including at least one said general purpose processor comprising a reduced instruction set computer processor.

However, Scales teaches a distributed computer system including a distributed shared memory (see abstract). Scales shows evidence of the use of a reduced instruction set computer processor (col. 1, lines 63-67; col. 2, lines 1-7, 49-67; col. 3, lines 1-8, 41-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Irwin and Kadambi in view of Scales to use a reduced instruction set

computer processor. One would be motivated to do so because a reduced instruction set processor allows for rapid execution of a sequence of simple instructions.

(10) Response to Argument

The Examiner summarizes various points raised by the Appellant and addresses replies individually.

With regards to Issue #1, Group #1: Claim 1 of the appeal brief, the Appellant argues that Irwin does not disclose "a first data processing unit adapted to filter incoming packets", "a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit", and "a data bus connecting the addressable memory unit and the first and second data processing units."

In response, the Examiner respectfully disagrees:

The Appellant states that the procedures for forwarding a data packet, in Irwin, fail to suggest filtering incoming packets. As seen in column 5, lines 47-65, the forwarding program determines the outgoing route to be followed by a data packet. The definition of filtering is a device or program that separates data, which is exactly what the forwarding of Irwin is doing. The packets are forwarded to different routes, thus being separated, which is the very definition of filter. The data packet processing

system, on column 6, lines 5-8, assigns a program counter to incoming packets and forwards them using the forwarding program; thus Irwin clearly teaches "a first data processing unit adapted to filter incoming packets." The Appellant also relies on column 1, lines 32-57 of Irwin to show that the limitation is not found, but the Examiner would like to point out, regardless, that portion of Irwin refers to figure 1 which is labeled as prior art. Even so, it teaches forwarding through different interfaces which is clearly filtering.

The Appellant also states that "a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit" is not found in Irwin. As seen in column 6, lines 5-16, a thread is assigned to the packet by the data packet processing system, which is the first data processing unit of the claim. The second data processing unit is in the process followed after the packet process. This second data processing unit uses the thread which is represented by a thread identification number. Thus, column 6, lines 5-16, clearly teaches the third limitation of claim 1.

In addition, the Appellant states that “a data bus connecting the addressable memory unit and the first and second data processing units" is not found in Irwin. The Examiner pointed to column 8, lines 49-52 to show that a data bus is explicitly shown in the reference. There is also a processor bus shown on column 7, lines 49-52. Regardless, it is clear from reading column 6, lines 5-16, that the addressable memory unit and first and second processing units are connected by a data bus as they all load

data and data is transferred from one to another and thus must be connected by a data bus. The data bus is inherently necessary.

With regards to Issue #2, Group #1: Claims 2 and 16 of the appeal brief, the Appellant argues that the claims are not met by the prior art for the reasons argued with respect to Issue #1, Group #1. Accordingly, there are no arguments for the Examiner to respond to with respect to this section of the Appeal Brief.

With regards to Issue #2, Group #2: Claims 3, 5, 13, and 14 of the appeal brief, the Appellant argues that Irwin and Kadambi do not disclose "a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy."

In response, the Examiner respectfully disagrees:

The portion of Irwin used in the rejection, column 1, lines 32-57, is there to show the use of a table for routing. All of claim 3 is found in the 103 reference, Kadambi. It appears the Appellant does not provide arguments other than stating that the portions relied on in Kadambi do not disclose the claim. The Examiner disagrees as seen in column 35, lines 57-64, which teaches a rules table that stores the filtering logic used to take appropriate action with. The rules table is equivalent to a policy action table as the filtering logic is a data processing policy. The filtering logic is a processing policy because it has policies for packet processing as evidenced by the various processing actions the filtering logic can perform. Thus, “a policy action table connected to said

data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy" is clearly disclosed in combination of Irwin and Kadambi.

With regards to Issue #2, Group #3: Claim 4 of the appeal brief, the Appellant argues that Irwin and Kadambi do not disclose "a first address pointer element for identifying the location in said addressable memory unit of one of said plurality of instruction sets" and "a second address pointer element for identifying the location in said addressable memory unit of a state block."

In response, the Examiner respectfully disagrees:

The Appellant continues to provide no arguments and only states that the art does not disclose the claim. There is no explanation as to why the Appellant disagrees with the Examiner's rejection. Regarding the first limitation, column 35, lines 57-64, Kadambi discloses logic 1411 in the FFP 141 which points to instruction sets to take action. Regarding the second limitation, column 31, lines 20-34, Kadambi discloses the FFP which is essentially a state machine. Irwin discloses the addressable memory unit in claim 1. Thus, it is shown that Kadambi combined with Irwin discloses these limitations.

With regards to Issue #2, Group #4: Claims 6-12 of the appeal brief, the Appellant argues that Irwin and Kadambi do not disclose "wherein said first data processing unit comprises logic for matching a first incoming packet to a stored first rule

and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table."

In response, the Examiner respectfully disagrees:

Once again, the Appellant does not provide any arguments and only states that the art does not disclose the claim. There is no explanation as to why the Appellant disagrees with the Examiner's rejection. In column 35, lines 24-65, packets are tagged for processing if they match selected fields in a filter mask. The matched packets are applied to rules tables to determine which actions will be taken. The thread generation and assignment is shown in Irwin and the policy action table is shown in column 35 of Kadambi, both previous responses in this answer. Thus, the combination of Irwin and Kadambi discloses this group of claims.

With regards to Issue #2, Group #5: Claim 15 of the appeal brief, the Appellant argues that Irwin and Kadambi do not disclose "a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit."

In response, the Examiner respectfully disagrees:

In column 30, lines 54-66 of Kadambi there is the use of priority queues that temporarily store packets. In addition, column 10, lines 5-17, of Irwin discloses a data packet stored in a packet buffer before processing by the second data processing unit. Claim 15 is clearly shown in the combination of arts.

With regards to Issue #2, Group #6: Claim 30 of the appeal brief, the Appellant argues that Irwin and Kadambi do not disclose "a first data processing unit adapted to filter incoming packets", "a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit", "a data bus connecting the addressable memory unit and the first and second data processing units", "wherein a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy", "wherein said data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table", "wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet", "wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table", "wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to

temporarily store packets before processing by said second data processing unit", and "wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit, which is in turn coupled to the policy action table and the state block for generating an output."

In response, the Examiner respectfully disagrees:

Regarding the limitation, *"a first data processing unit adapted to filter incoming packets," t*he Appellant states that the procedures for forwarding a data packet, in Irwin, fail to suggest filtering incoming packets. As seen in column 5, lines 47-65, the forwarding program determines the outgoing route to be followed by a data packet. The definition of filtering is a device or program that separates data, which is exactly what the forwarding of Irwin is doing. The packets are forwarded to different routes, thus being separated, which is the very definition of filter. The data packet processing system, on column 6, lines 5-8, assigns a program counter to incoming packets and forwards them using the forwarding program; thus Irwin clearly teaches "a first data processing unit adapted to filter incoming packets." The Appellant also relies on column 1, lines 32-57 of Irwin to show that the limitation is not found, but the Examiner would like to point out, regardless, that portion of Irwin refers to figure 1 which is labeled as prior art. Even so, it teaches forwarding through different interfaces which is clearly filtering.

Regarding the limitation, *"a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit,"*

the Appellant also states that "a second data processing unit adapted to process incoming packets according to one of said plurality of instruction sets after the filtering, based on a thread assigned to the incoming packets by the first data processing unit" is not found in Irwin. As seen in column 6, lines 5-16, a thread is assigned to the packet by the data packet processing system, which is the first data processing unit of the claim. The second data processing unit is in the process followed after the packet process. This second data processing unit uses the thread which is represented by a thread identification number. Thus, column 6, lines 5-16, clearly teaches this limitation.

Regarding the limitation, *"a data bus connecting the addressable memory unit and the first and second data processing units,"* the Appellant states that "a data bus connecting the addressable memory unit and the first and second data processing units" is not found in Irwin. The Examiner pointed to column 8, lines 49-52 to show that a data bus is explicitly shown in the reference. There is also a processor bus shown on column 7, lines 49-52. Regardless, it is clear from reading column 6, lines 5-16, that the addressable memory unit and first and second processing units are connected by a data bus as they all load data and data is transferred from one to another and thus must be connected by a data bus. The data bus is inherently necessary.

Regarding the limitation, *"wherein a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy,"* column 35, lines 57-64, teaches a rules table that stores the filtering logic used to take appropriate action with. The rules table is equivalent to a policy action table as the filtering logic is a data processing policy. The filtering logic is

a processing policy because it has policies for packet processing as evidenced by the various processing actions the filtering logic can perform. Thus, "a policy action table connected to said data bus and said addressable memory unit, wherein said policy action table stores at least one data processing policy" is clearly disclosed in combination of Irwin and Kadambi.

Regarding the limitation, *"wherein said data processing unit comprises logic for matching a first incoming packet to a stored first rule and for generating a first thread if the first incoming packet matches said first rule, said first thread identifying the location of one of said at least one data processing policies in said policy action table",* column 35, lines 24-65, packets are tagged for processing if they match selected fields in a filter mask. The matched packets are applied to rules tables to determine which actions will be taken. The thread generation and assignment is shown in Irwin and the policy action table is shown in column 35 of Kadambi, both previous responses in this answer. Thus, the combination of Irwin and Kadambi discloses this limitation.

Regarding the limitation, *"wherein said data processing policy comprises a first address pointer to a starting address of a first set of instructions and a second address pointer to a starting address of a state block stored in said addressable memory unit, said state block used by said first set of instructions for processing the first incoming packet",* column 35, lines 57-64, Kadambi discloses logic 1411 in the FFP 141 which points to instruction sets to take action and, column 31, lines 20-34, Kadambi discloses the FFP which is essentially a state machine. Irwin discloses the addressable memory

unit and processing a first incoming packet and thus, it is shown that Kadambi combined with Irwin discloses this limitation.

Regarding the limitation, *"wherein said first processing unit further comprises logic for matching a second incoming packet to a stored second rule and for generating a second thread if the second incoming packet matches the second rule, said second thread identifying the location of one of said at least one data processing policy in said policy action table",* column 35, lines 24-65, packets are tagged for processing if they match selected fields in a filter mask. The matched packets are applied to rules tables to determine which actions will be taken. The multiple thread generation and assignment and multiple incoming packets is shown in Irwin and the policy action table is shown in column 35 of Kadambi, both previous responses in this answer. Thus, the combination of Irwin and Kadambi discloses this limitation.

Regarding the limitation, *"wherein a memory unit connected to said first data processing unit and to said second data processing unit, said memory unit adapted to temporarily store packets before processing by said second data processing unit",* column 5, lines 46-54, of Kadambi, teaches a pluarilty of systems and column 30, lines 54-66 teaches the use of priority queues that temporarily store packets. In addition, column 10, lines 5-17, of Irwin discloses a data packet stored in a packet buffer before processing by the second data processing unit. This limitation is clearly shown in the combination of arts.

Regarding the limitation, *"wherein the apparatus includes a control logic unit coupled to an input and the policy condition table for feeding an arithmetic logic unit,*

which is in turn coupled to the policy action table and the state block for generating an output," column 31, lines 20-34, of Kadambi, teaches a rules engine attached to FFP; column 35, lines 57-64, teaches filtering logic in a rules table; and column 31, lines 20-34, teach a FFP which is eventually a state machine for generating an output. These sections of Kadambi combined with the main reference of Irwin disclose this limitation.

As shown above, the combination of Irwin and Kadambi disclose all limitations of claim 30.

With regards to Issue #3, Group #1: Claims 17 and 18 of the appeal brief, the Appellant argues that the claims are not met by the prior art for the reasons argued with respect to Issue #2, Group #1. Accordingly, there are no arguments for the Examiner to respond to with respect to this section of the Appeal Brief.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Avi Gold/

Examiner, Art Unit 2157

Conferees:

/Yves Dalencourt/

Primary Examiner, Art Unit 2157

/Ario Etienne/

Supervisory Patent Examiner, Art Unit 2157